Customer No.: 31561
Docket No.: 12336-US-PA
Application No.: 10/710,662

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-20. Specifically, the Office Action rejected claims 1-6, 8-14 and 16-20 under 35 U.S.C. 102(b), as being anticipated by Abercrombie (US 5,798,568). The Office Action also rejected claims 7 and 15 under 35 U.S.C. 103(a) as being unpatentable over Abercrombie (US 5,798,568) in view of Sugahara (U.S. 5,401,683).

No claim is amended. Claims 1-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Rejections under 102(b)

Applicant respectfully traverses the 102(b) rejection of claims 1-6, 8-14 and 16-20 because Abercrombie (US 5,798,568) does not teach every element recited in these claims.

> In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co.,

868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

The present invention is related to a stress relieving method as claim 1 recites:

Claim 1. A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area ***such that at least no circuits are formed on the dielectric layer within the first area***;

forming a plurality of first openings in the dielectric layer within the first area; and

forming a first material layer over the wafer, wherein the upper surface of the first material layer has pits at locations over the first openings.

The office action stated Abercrombie has disclosed the limitation of the wafer is divided into a first area (reference 11) and a second area (reference 12 and 13) such that at least no circuits are formed on the dielectric layer within the first area in Fig. 3. However, applicant disagrees. As a matter of fact, if reference 11 is as the first region and reference 12 and 13 are as the second region, there is **a circuit (reference 15)** formed on the dielectric layer (reference 14) within the first area (reference 11).

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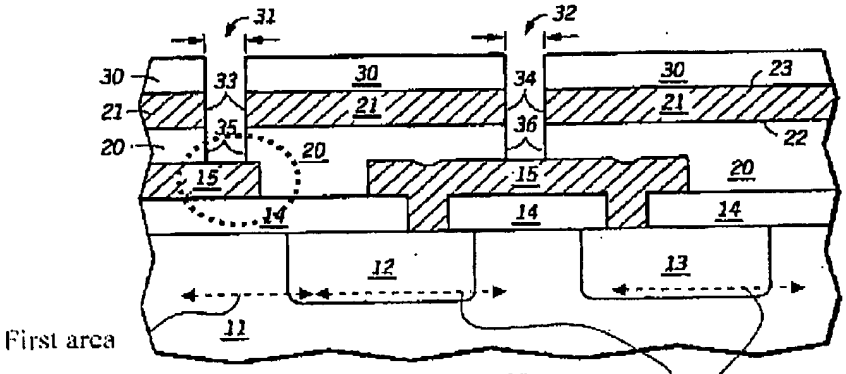

FIG. 3

The office action also stated Abercrombie has disclosed the limitation of forming a plurality of first openings in the dielectric layer within the first area (Fig. 3, reference 14; col. 2, lines 50-51). However, applicant disagrees. Abercrombie teaches layer 14 has vias exposing contact portions of device 12 and 13 at col. 2, lines 50-51. Apparently, the vias are formed within the second area (reference 12 and 13) but not within the first area (reference 11).

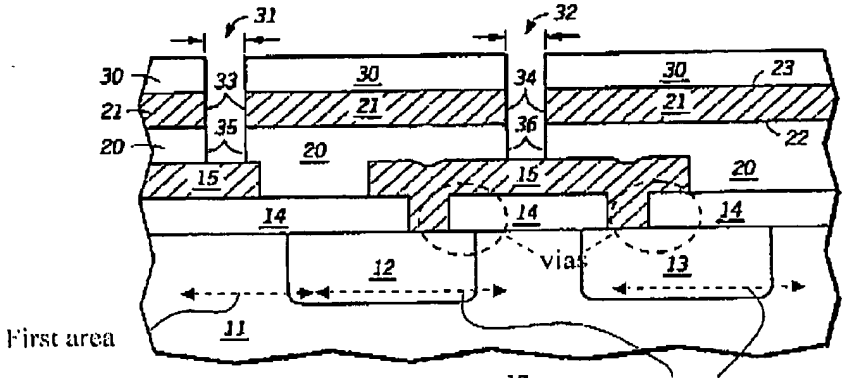

FIG.3

Therefore, applicant respectfully submits Abercrombie fails to teach or suggest the limitations of the wafer is divided into a first area and a second area such that at least ***no circuits are formed on the dielectric layer within the first area*** and ***forming a plurality of first openings in the dielectric layer within the first area.*** Abercrombie does not teach every element recited in claim 1. Applicant respectfully submits that independent claim 1 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 2-6, 8-9 and 19 patently define over the prior art as well.

In particular, regarding to claims 2 and 4, the office action stated Abercrombie has disclosed the first area comprises a scribe line at col. 1, lines 56-67 thru col. 2, lines 1-18. However, applicant respectfully submits Abercrombie just teaches "the scribe lines between integrated circuits or other key/alignment mark locations on the wafer are cleared .....". Abercrombie does not teach the scribe lines are formed in the first area as claims 2 and 4

recite.

The present invention also provides a stress relieving method as claim 10 recites:

Claim 10. A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein ***the wafer is divided into a first area and a second area such that no circuits are formed within the first area;***

forming a first material layer over the wafer,; and

removing a portion of the first material layer within the first area to form a plurality of first openings.

The office action stated Abercrombie has disclosed the limitation of the wafer is divided into a first area (reference 11) and a second area (reference 12 and 13) such that at least no circuits are formed on the dielectric layer within the first area in Fig. 3. As discussed above, if reference 11 is as the first region and reference 12 and 13 are as the second region, there is **a circuit (reference 15)** formed on the dielectric layer (reference 14) within the first area (reference 11). Therefore, applicant respectfully submits Abercrombie fails to teach or suggest the limitations of the wafer is divided into a first area and a second area such that at least ***no circuits are formed on the dielectric layer within the first area*** as claim 10 recites.

In addition, the office action also stated Abercrombie has disclosed the limitation of removing a portion of the first material layer (reference 15) within the first area to form a plurality of first openings in Fig. 1 (reference 16). However, applicant disagrees. As a matter of fact, the opening shown in Fig. 1 is formed within the first area and second area (most portion of the opening is formed within the second area), but not only formed within the first area.

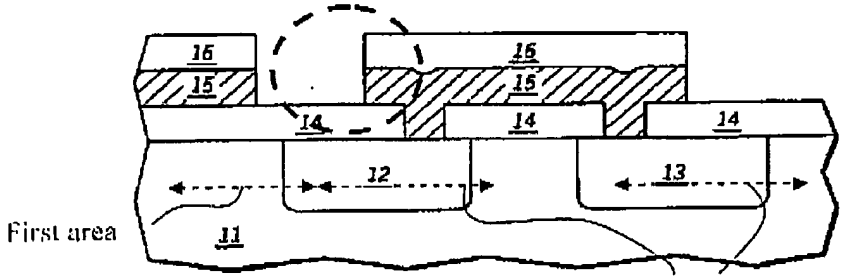

FIG.1

For at least the foregoing reasons, applicant respectfully submits Abercrombie fails to teach or suggest the limitations of the wafer is divided into a first area and a second area such that at least ***no circuits are formed on the dielectric layer within the first area*** and ***removing a portion of the first material layer within the first area to form a plurality of first openings*** as claim 10 recites. Abercrombie does not teach every element recited in claim 10. Applicant respectfully submits that independent claim 10 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent

claims 11-14 and 16-18 and 20 patently define over the prior art as a matter of law.

In particular, regarding to claims 11 and 13, the office action stated Abercrombie has disclosed the first area comprises a scribe line at col. 1, lines 56-67 thru col. 2, lines 1-18. However, applicant respectfully submits Abercrombie just teaches "the scribe lines between integrated circuits or other key/alignment mark locations on the wafer are cleared .....". Abercrombie does not teach the scribe lines are formed in the first area as claims 11 and 13 recite.

Rejections under 103(a)

The Office Action rejected claims 7 and 15 under 35 U.S.C. 103(a), as being unpatentable over Abercrombie (US 5,798,568) in view of Sugahara (U.S. 5,401,683). Applicant respectfully traverses the rejections for at least the reasons set forth below.

> To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner

resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

Applicants submit that, as discussed above, Abercrombie fails to teach or suggest each and every element of claims 1, 10, from which claims 7 and 15 depend. Sugahara also fails to teach or suggest the wafer is divided into a first area and a second area such that at least ***no circuits are formed on the dielectric layer within the first area*** and ***forming a plurality of first openings in the dielectric layer within the first area*** as claim 1 recites. Sugahara also fails to teach or suggest the wafer is divided into a first area and a second area such that at least ***no circuits are formed on the dielectric layer within the first area*** and ***removing a portion of the first material layer within the first area to form a plurality of first openings*** as claim 10 recites

Sugahara cannot cure the deficiencies of Abercrombie. Therefore, independent claims 1 and 10 are patentable over Abercrombie and Sugahara. For at the least the same reasons, their dependent claims 7 and 15 are also be patentable as a matter of law.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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